CS 201 Lecture 4
Decoders, Multiplexers, ALUs

Spring 2014
Plan today

- Decoders
- Multiplexers
- Arithmetic-Logic Units
Decoders

- Some number \( N \) of select lines
- \( 2^N \) output lines
- Line \( x \) is selected when the inputs encode the unsigned binary number for \( x \)

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Example Implementation (2 to 4)
Fun with Decoders

• Implement any n-bit binary function with an n-bit decoder and one extra gate
What does this circuit do?
Multiplexer (MUX)

- Used for selection
- Choose one of several inputs to pass along to output
- N select bits, $2^N$ inputs
- X-to-1 MUX means we are selecting from among X inputs
Fun with MUXs

• Handout
Arithmetic Logic Unit

- A controllable hardware unit that will perform a variety of operations based on control signals
- Inputs: two numbers A and B
- Control signals choose desired operation
- Output is the chosen operation applied to inputs
- More in lab tomorrow