High-Radix On-chip Networks with Low-Radix Routers

Ridham Dholaria & Pedro Lopez Vargas

I. INTRODUCTION

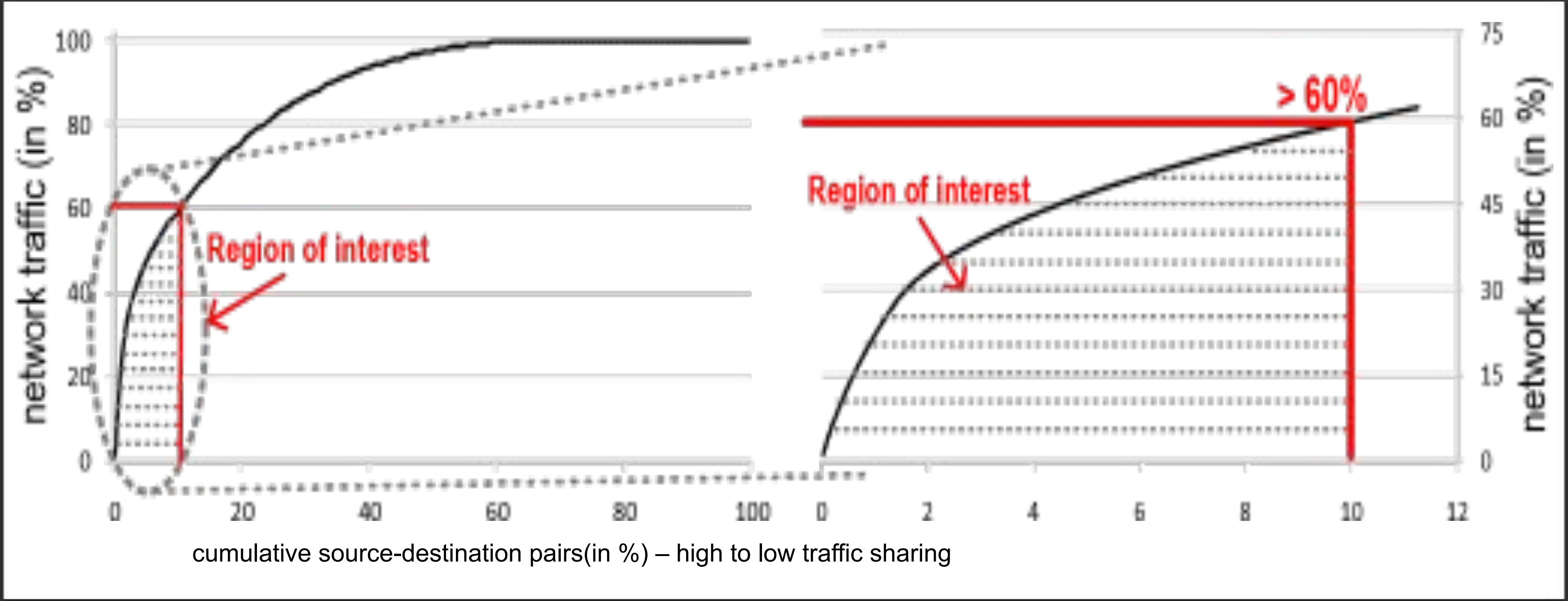
The radix of the network routers is a **key design** choice : -

➔ **High-radix routers have low-diameter topologies**
Increasing signal propagation latencies and slower operating frequencies

➔ **Low-radix routers have high-diameter topologies**
They operate at higher frequencies and use less area and power but can lead to large network diameters and high hop counts

➔ **HiROIC (High Radix On-chip Networks at Incremental re-configuration Cost) is proposed**
Optimize connectivity for high-volume source-destination pairs

Relationship between Network Traffic and Source-destination pairs



Network activity shared by the most exercised source-destination pairs.

II. RELATED WORK

- ➔ **Design time**
  During the design process
  - Optimizing router design for specific topologies and flow control.
- ➔ **HiROIC**
  During run-time

III. METHODOLOGY

To optimize the topology for high-volume communication patterns, we perform the following steps:

- ➔ **Collect traffic statistics over execution intervals (epochs) to predict future traffic behavior**
- ➔ **We trigger topology reconfigurations when we observe pattern changes**
- ➔ **We set port-link bindings at each router based on the new topology planned.**

HiROIC's Execution Flow

Distributed traffic statistics collection framework monitors the density of communication between all source-destination pairs.

Goal is to identify the pairs that transfer the majority of the traffic so as to minimize their hop count.

Note

Networks-on-chip (NoCs) are is a network-based communications subsystem

IV. TOPOLOGY RECONFIGURATION

The authors implemented a distributed, deadlock-free reconfiguration algorithm to predict the future communication needs of applications and optimize the network topology based on these needs.

- ➔ **Monitoring**
  traffic patterns
- ➔ **Determine**
  whether a reconfiguration is necessary
- ➔ **Adjust**
  connections between routers and links in architecture

V. HARDWARE ADDITIONS

The HiROIC hardware implementation consists of five components at each router : -

- ➔ A directory to maintain per-destination traffic statistics
- ➔ A reconfiguration-trigger unit
- ➔ A distributed constraint checker (CC)
- ➔ An exception-handling unit
- ➔ A threshold-update unit

VI. PHYSICAL TOPOLOGIES

➔ **2D Mesh:** 5.A

➔ **Adaptive 3D Torus:** 5.B

➔ **Adaptive Flattened Butterfly:** 5.C

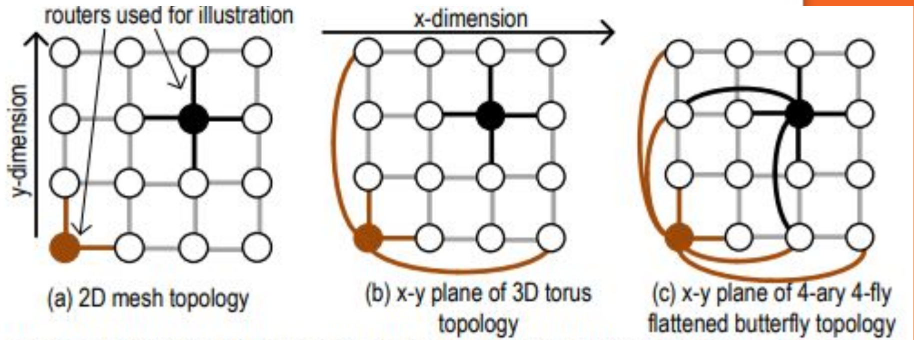


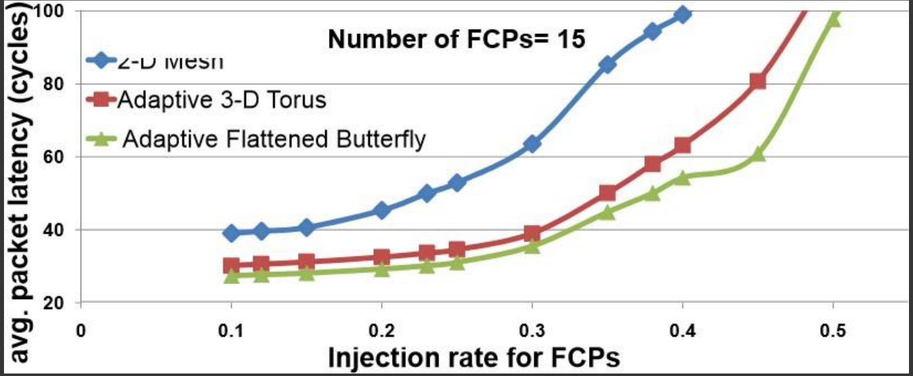
Fig. 5: **Organization of links and routers in proposed physical topologies.** We consider two topologies for links: a 3D torus and a flattened butterfly. Routers are organized as in a 2D mesh. For simplicity of illustration, the figure shows the x- and y- dimension connections only for the bold colored routers. 3D torus routers have two connections in each dimension, while a 4-ary 4-fly flattened butterfly has three per dimension.

VII. EXPERIMENTAL RESULTS

A. Synthetic Traffic
B. Multiprogrammed Workloads
C. Area and Power Overhead

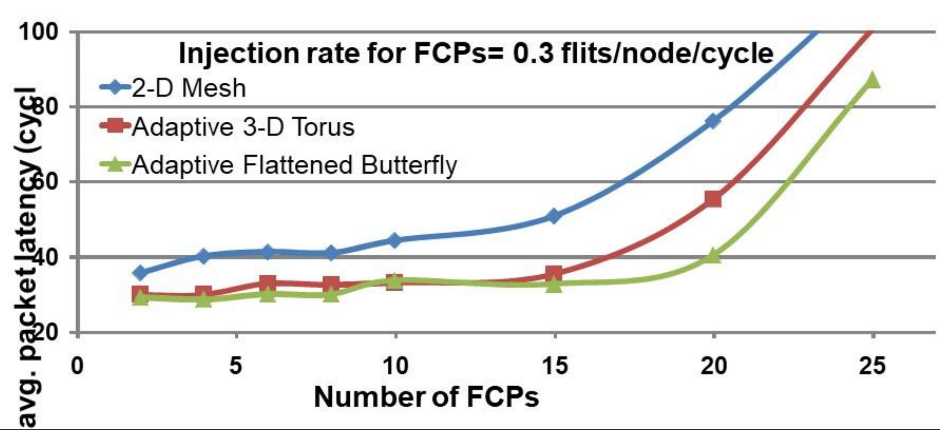
Average Network latency

Note: FCP - Frequently Communicating Pair



Directed traffic

Varying number of FCPs



VIII. CONCLUSION

Keynotes to take home : -

- **A router architecture to mimic the high-radix routers' connectivity while consuming resources comparable to a low-radix router.**
- **Deadlock-free reconfiguration algorithm**
  Predict an application's future communication needs and optimize the network topology to provide short paths between high-traffic source- destination pairs.
- **HiROIC (High Radix On-chip Networks at Incremental re-configuration Cost) is proposed**
  Optimize connectivity for high-volume source-destination pairs